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upon reset. Also, the SP is pre-incremented for push

operations and post-decremented for pop operations. The

first write to the stack following a system reset (assuming the

SP is left as is) is to location 08H, and the second is to

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Appendix A describes each 8051 instruction in detail, with examples. Appendix A also provides the clock count for instructions, 8051 register diagrams, and RAM memory maps. Appendix B describes basics of wire wrapping. Appendix C covers IC technology and logic families, as well as 8051 I/O port interfacing and fan-out.

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